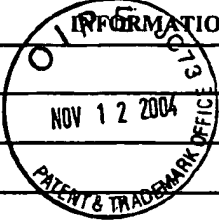
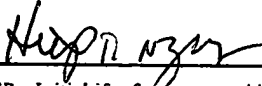
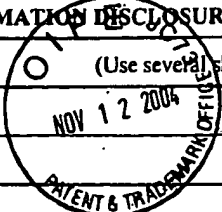


U.S. Department of Commerce, Patent and Trademark Office						Attorney Docket No.: 023-0001		
						Application No.: 09/990,901		
 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)						Applicant(s): Roy Scheuerlein		
						Filing Date: Nov. 16, 2001		
						Group Art Unit: 2818		
						Date Submitted: January 3, 2002		
U.S. Patent Documents								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
HJ	AA	4,646,266	Feb. 24, 1987	Ovshinsky et al.	365	105		
	AB	5,109,360	Apr. 28, 1992	Inazumi et al.	365	200		
	AC	5,172,341	Dec. 15, 1992	Amin	365	222		
	AD	5,315,558	May 24, 1994	Hag	365	230.01		
	AE	5,367,653	Nov. 22, 1994	Coyle et al.	395	400		
	AF	5,671,229	Sep. 23, 1997	Harari et al.	371	10.2		
	AG	5,691,945	Nov. 25, 1997	Liou et al.	365	200		
	AH	5,751,012	May 12, 1998	Wolstenholme et al.	257	5		
	AI	5,764,576	Jun. 9, 1998	Hidaka et al.	365	200		
	AJ	5,805,520	Sep. 8, 1998	Anglada	365	230.02		
V	AK	5,835,396	Nov. 10, 1998	Zhang	365	51		
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							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AL							
	AM							
	AN							
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OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
HJ	AR	U.S. App. No. 09/748,649, filed Dec. 22, 2000, "Partial Selection of Passive Element Memory Cell Sub-Arrays for Write Operations," inventors Roy E. Scheuerlein and Matthew P. Crawley, 38 pp.						
	AS	U.S. App. No. 09/897,705, filed June 29, 2001, "Three-Dimensional Memory Array Incorporating Serial Chain Diode Stack," inventors Bendik Kleveland et al., 72 pp.						
	AT	U.S. App. No. 09/747,574, filed Dec. 22, 2000, entitled "Three-Dimensional Memory Array and Method for Storing Data Bits and ECC Bits Therein," and naming inventors Thomas H. Lee, James M. Cleaves and Mark G. Johnson, 18 pages.						
Examiner								
		Date Considered 3/3/05						
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H2	AA	5,896,404	Apr. 20, 1999	Kellogg et al.	371	40.11		
	AB	5,999,446	Dec. 7, 1999	Harari et al.	365	185.03		
	AC	6,020,758	Feb. 1, 2000	Patel et al.	326	40		
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H2 ↓	AR	U.S. Pat. App. No. 09/560,626, filed April 28, 2000, entitled "Three-Dimensional Memory Array and Method of Fabrication," naming inventor N. Johan Knall, 48 pp.						
	AS	U.S. App. No. 09/638,428, filed Aug. 14, 2000, "Low Cost Three-Dimensional Memory Array," inventors Mark G. Johnson et al., 25 pp.						
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Examiner <i>Hiep Nguyen</i>		Date Considered <i>3/3/05</i>						

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					Date Submitted: January 3, 2002			
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H2	AA	6,166,559	Dec. 26, 2000	McClintock et al.	326	10		
	AB	6,192,487 B1	Feb. 20, 2001	Douceur	714	8		
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							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
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	AS	Kim C. Hardee and Rahul Sud, "A Fault-Tolerant 30 ns/375 mW 16K x 1 NMOS Static RAM," IEEE Journal of Solid-State Circuits, Vol. SC-16, No. 5, Oct. 1981, pp. 435-443.						
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↓	AU	"TH58512FT Toshiba MOS Digital Integrated Circuit Silicon Gate CMOS" datasheet, 1999, 34 pp.						
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